Sub-1 GHz RF Narrowband Transceiver Module

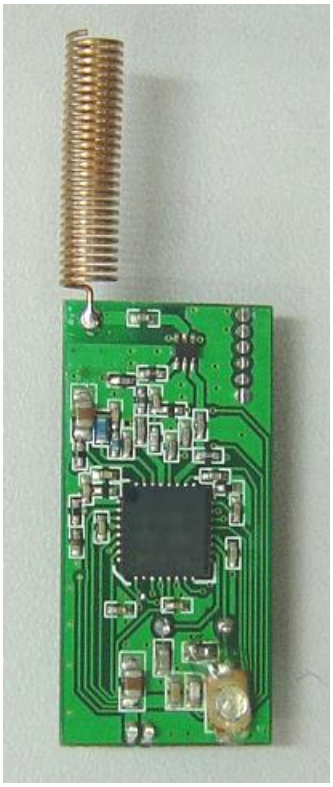
Description

The EBWISE **MO-CC1120** RF module is a high performance low power RF transceivers designed for operation with a companion MCU. The module has built-in TI **CC1120 chip** which fully integrated single-chip radio transceiver designed for high performance at very low-power and low-voltage operation in cost-effective wireless systems. All filters are integrated, thus removing the need for costly external SAW and IF filters. The device is mainly intended for Industrial, Scientific, and Medical (ISM) applications and Short Range Device (SRD) frequency bands at 164 to 192 MHz, 274 to 320 MHz, 410 to 480 MHz, and 820 to 960 MHz.

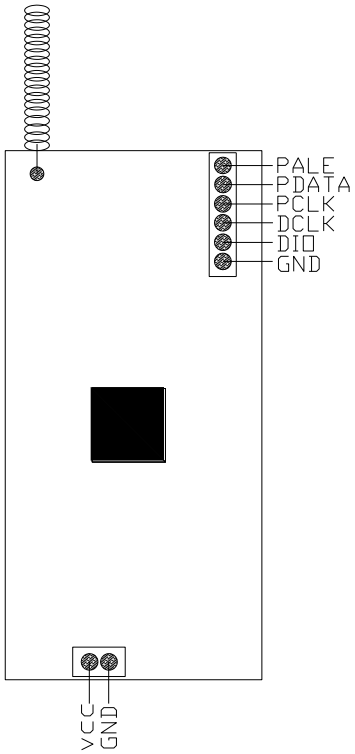
Key Features

- High-Performance Single-Chip Transceiver.
  - Adjacent Channel Selectivity: 64 dB at 12.5-kHz Offset
  - Blocking Performance: 91 dB at 10 MHz
  - Excellent Receiver Sensitivity:
    - –123 dBm at 1.2 kbps
    - –110 dBm at 50 kbps
    - –127 dBm Using Built-in Coding Gain
  - Very Low Phase Noise:
    –111 dBc/Hz at 10-kHz Offset
- Suitable for Systems Targeting ETSI Category 1 Compliance in 169-MHz and 433-MHz Bands
- High Spectral Efficiency (9.6 kbps in 12.5-kHz Channel in Compliance With FCC Narrowbanding Mandate)
- Separate 128-Byte RX and TX FIFOs
- Wide Supply Voltage Range (2.0 V to 3.6 V)
- Programmable Output Power up to +16 dBm With 0.4-dB Step Size
- Configurable Data Rates: 0 to 200 kbps
- Supported Modulation Formats: 2-FSK, 2-GFSK, 4-FSK, 4-GFSK, MSK, OOK
- Support for Automatic Acknowledge of Received Packets

Module



PIN Diagram



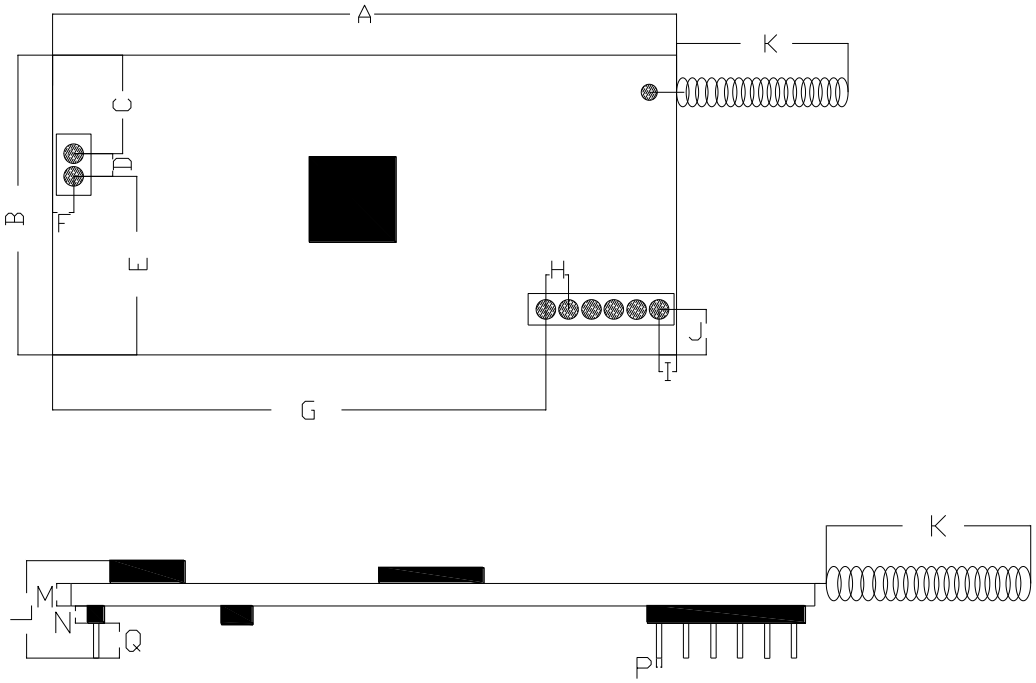
Pin Descriptions

Pin No	Pin Name	Pin Type	Description
	VCC	Power	2.0V - 3.6V power 2.0V ~ 3.6V
	GND	Ground	GND
	DIO	Digital input/output	Data input in transmit mode; data output in receive mode Can also be used to start power-up sequencing in receive
	DCLK	Digital output	Clock for data in both receive and transmit mode. Can be used as receive data output in asynchronous mode
	PCLK	Digital input	Programming clock for SPI configuration interface
	PDATA	Digital input/output	Programming data input for SPI configuration interface Programming data output for SPI configuration interface
	PALE	Digital input	Programming chip select, active low, for configuration interface.

Absolute Maximum Ratings

Parameter	Rating	Units
Supply Voltage	2.0~3.6	V DC
Operating Temperature	-40 to +85	℃

Package Description



Name	Dimension	Name	Dimension	Name	Dimension
A	35mm+-0.5mm	**G**	27.7mm+-0.2mm	**M**	1mm+-0.1mm
B	16.8mm+-0.2mm	**H**	1.27mm	**N**	2.5mm+-0.2mm
C	5.5mm+-0.1mm	**I**	1mm+-0.1mm	**P**	0.45mm+-0.05mm
D	1.27mm	**J**	2.5mm+-0.1mm	**Q**	2.5mm+-0.1mm
E	10mm+-0.1mm	**K**	21mm(Max)		
F	1.2mm+-0.1mm	**L**	8.0mm (Max)		

RF receiver section

Tc = 25°C, VDD = 3V

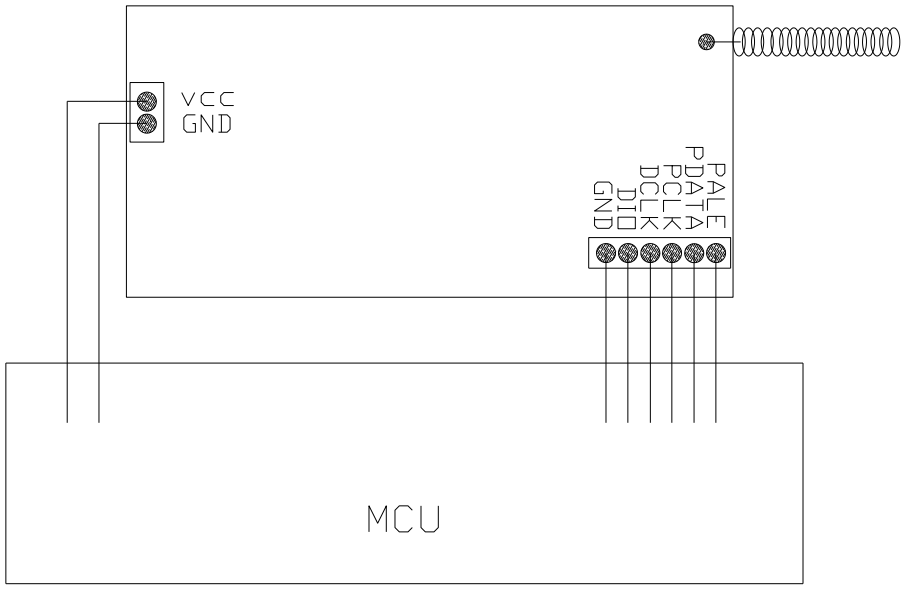
Parameter	Min	Typ	Max	Unit	Condition/Note
Receiver sensitivity		–120		dBm	2-FSK, 1.2kbps, 4kHz deviation, , 1% packet error rate, 20 bytes packet length, 10kHz digital channel filter bandwidth
		-106		dBm	50 Kbps,2GFSK,25kHz deviation, 1% packet error rate, 20 bytes packet length, 100 kHz digital channel filter bandwidth
Saturation		+10		dBm	
Digital channel filter bandwidth	8		200	kHz	User programmable. The bandwidth limits are proportional to crystal frequency (given values assume a 32 MHz crystal).

RF Transmit Section

Tc = 25°C, VDD =3.0V

Parameter	Min	Typ	Max	Unit	Condition/Note
Output power, highest setting		15		dBm	Output power is programmable, and full range is available in all frequency bands.

Application Circuit



Module Program

1. Configuration Software

CC112X can be configured using the SmartRF™ Studio software (SWRC046). SmartRF Studio is highly recommended for obtaining optimum register settings, and for evaluating performance and functionality.

After chip reset, all registers have default values and these might differ from the optimum register setting. It is therefore necessary to configure/reconfigure the radio through the SPI interface after the chip has been reset. SmartRF Studio provides a code export function making it easy to implement this in firmware.

2. Microcontroller Interface

➢ **Configuration**

In a typical system, CC1120 will interface to an MCU. This MCU must be able to communicate with the CC1120 over a 4-wire SPI interface to be able to:

- Configure the CC1120
- Program CC1120 into different modes (RX, TX, SLEEP, IDLE, etc)
- Read and write buffered data (RX FIFO and TX FIFO)
- Read status information

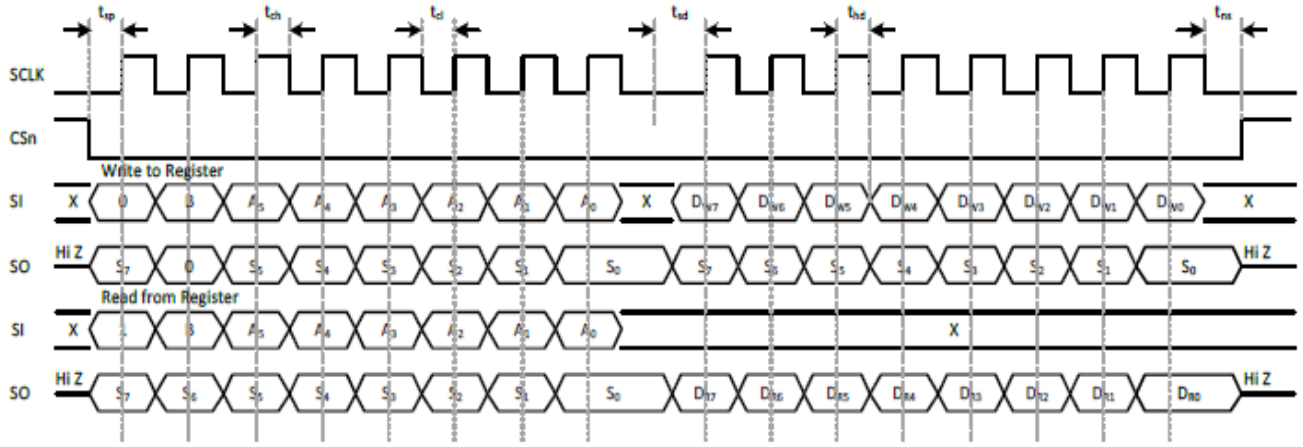
➢ **4-wire Serial Configuration and Data Interface**

CC1120 is configured via a simple 4-wire SPI-compatible interface (SI, SO, SCLK, and CSn) where CC1120 is the slave. This interface is also used to read and write buffered data. All transfers on the SPI interface are done most significant bit first.

All transactions on the SPI interface start with a header byte containing a R/$\overline{W}$ bit, a burst access bit(B), and a 6-bit address (A_5 - A_0). A status byte is sent on the SO pin each time a header byte istransmitted on the SI pin (see Section 3.1.2 for more details on the chip status byte).

The CSn pin must be kept low during transfers on the SPI bus. The timing for the address and data transfers on the SPI interface is shown in below picture 1 with reference to below Figure 1.

✧ **Figure 1**



✧ **Table 1**

Parameter	Description	Min		Max		Units
f_{SCLK}	SCLK frequency read/write access Note: 100 or 125 ns delay between consecutive data bytes must be added during burst write access to the configuration registers depending on f_{XOSC} (40 or 32 MHz)	-		10	f_{XOSC} = 40 MHz	MHz
				8	f_{XOSC} = 32 MHz	
	SCLK frequency read access extended memory	-		7.7	f_{XOSC} = 40 MHz	
				6.1	f_{XOSC} = 32 MHz	
t_{sp}	CSn low to positive edge on SCLK	50		-		ns
t_{ch}	Clock high	47.5	f_{XOSC} = 40 MHz	-		ns
		60	f_{XOSC} = 32 MHz			
t_{cl}	Clock low	47.5	f_{XOSC} = 40 MHz	-		ns
		60	f_{XOSC} = 32 MHz			
t_{rise}	Clock rise time	-		40		ns
t_{fall}	Clock fall time	-		40		ns
t_{sd}	Setup data before a positive edge on SCLK	10		-		ns
t_{hd}	Hold data after positive edge on SCLK	10		-		ns
t_{ns}	Negative edge on SCLK to CSn high.	200		-		ns
	CSn high time, time from CSn has been pulled high until it can be pulled low again	50				ns

3. Modulation Formats

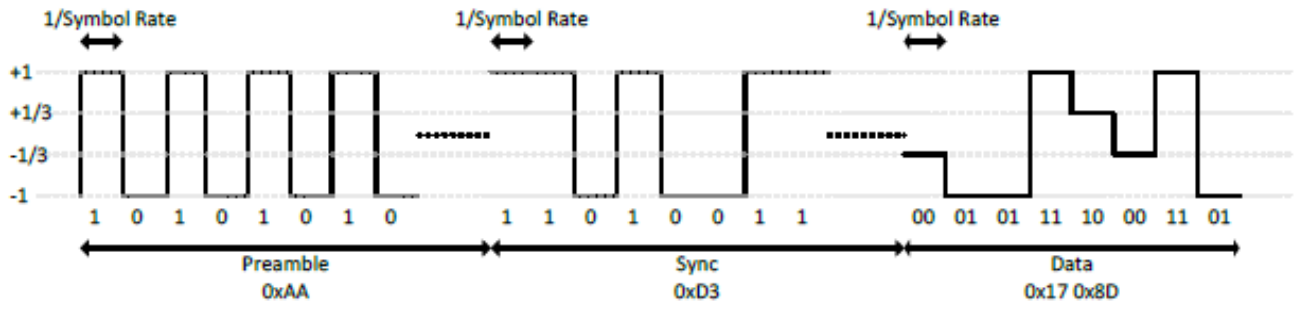
CC112X supports amplitude and frequency shift modulation formats. The desired modulation format is set in the MODCFG_DEV_E.MOD_FORMAT register.

Optionally, the data stream can be Manchester encoded by the modulator and decoded by the demodulator. This option is enabled by setting MDMCFG1.MANCHESTER_EN = 1. Note that Manchester encoding/decoding is only performed on the payload (including optional length and address field) and the CRC and that all packet handling features are still available. In applications where preamble and sync word also need to be Manchester encoded, this can be achieved by selecting PREAMBLE_CFG1.PREAMBLE_WORD = 10_b or 11_b and manually encoding a two byte long sync word and write it to SYNC3/2/1/0

3.1 Frequency Shift Keying

CC112X supports both 2-FSK and 4-FSK modulation. Both can optionally be shaped by a Gaussian filter with BT = 0.5, producing a GFSK modulated signal. This spectrum-shaping feature improves adjacent channel power (ACP) and occupied bandwidth. When selecting 4-(G)FSK, the preamble and sync word is sent using 2-(G)FSK (see below Figure 2).

➢ Figure 2



In ‘true’ 2-FSK systems with abrupt frequency shifting, the spectrum is inherently broad. By making the frequency shift ‘softer’, the spectrum can be made significantly narrower. Thus, higher symbol rates can be transmitted in the same bandwidth using GFSK.

When 2-(G)FSK/4-(G)FSK modulation is used, the DEVIATION_M and MODCFG_DEV_E.DEV_E register specifies the expected frequency deviation of incoming signals in RX and should be the same as the TX deviation for demodulation to be performed reliably and robustly.

The frequency deviation is programmed with the DEV_M and DEV_E values in the DEVIATION_M and MODCFG_DEV_E.DEV_E register. The value has an exponent/mantissa form, and the resultant deviation is given by Equation 1 and Equation 2.

$$f_{dev} = \frac{f_{xosc}}{2^{24}} \cdot (256 + DEV\_M) \cdot 2^{DEV\_E} \text{ [Hz]}$$

Equation 1: f_{dev} (DEVIATION_E > 0)

$$f_{dev} = \frac{f_{xosc}}{2^{23}} \cdot DEV\_M \text{ [Hz]}$$

Equation 2: f_{dev} (DEVIATION_E = 0)

The symbol encoding can be configured through the `CFM_DATA_CFG.SYMBOL_MAP_CFG` register field as shown in below Table 2 (`SYMBOL_MAP_CFG = 0` by default).

✧ **Table 2**

Format	Symbol	Coding			
		SYMBOL_MAP_CFG = 00_b	SYMBOL_MAP_CFG = 01_b	SYMBOL_MAP_CFG = 10_b	SYMBOL_MAP_CFG = 11_b
2-(G)FSK OOK/ASK	‘0’	−Deviation [A_{Min}]	+Deviation [A_{Max}]	+Deviation[A_{Max}]	+Deviation [A_{Max}]
	‘1’	+Deviation [A_{Max}]	−Deviation [A_{Min}]	−Deviation [A_{Min}]	−Deviation [A_{Min}]
4-(G)FSK	‘00’	−Deviation /3	−Deviation	+Deviation /3	+Deviation
	‘01’	−Deviation	−Deviation /3	+Deviation	+Deviation /3
	‘10’	+Deviation /3	+Deviation	−Deviation /3	−Deviation
	‘11’	+Deviation	+Deviation /3	−Deviation	−Deviation /3

For the detail information, please link as below for design reference.
http://www.ti.com/lit/ug/swru295e/swru295e.pdf

Ordering Information:

Model Numbers	Frequency Ranges	Descriptions
MO-CC1120-434A	400MHz~464MHz	
MO-CC1120-868A	830MHz~900MHz	

Note : For detailed chip information, please see TI CC1120 data sheet .

TI WEB: www.ti.com