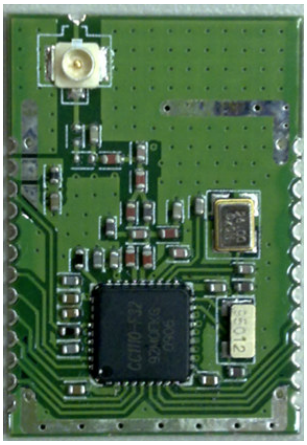
MO-CC1110F32

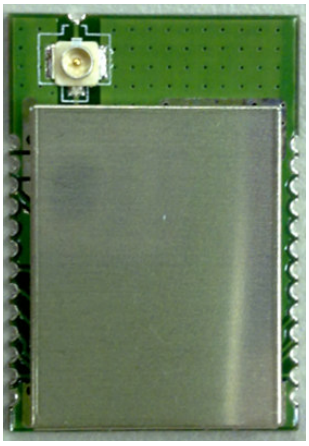
Low-Power SoC with Sub-1 GHz RF Transceiver module

Description

The EBWISE MO-CC1110F32 RF module is a true low-power sub-1 GHz system-on-chip (SoC) designed for low power wireless applications. The module has built-in TI **CC1110F32 chip** which combines the excellent performance RF transceiver and 8051 base MCU, with 32 kB programmable flash memory and 4 kB of RAM,

The core RF IC **CC1110F32** is highly suited for systems where very low power consumption is required. This is ensured by several



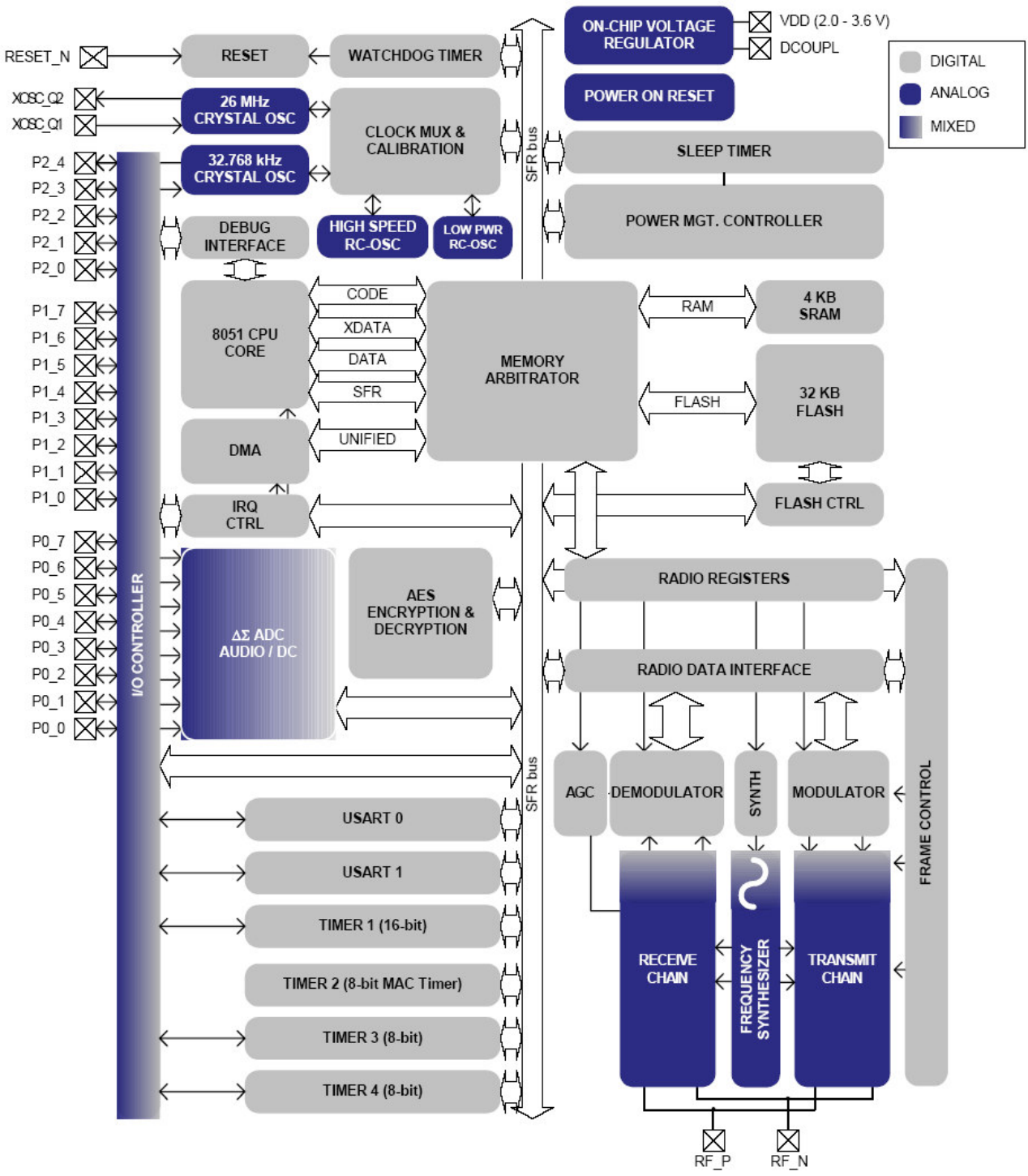


Key Features Radio

- High-performance RF transceiver based on the market-leading **CC1101**
- High sensitivity (–110dBm at 1.2 kBaud)
- Programmable data rate up to 500 kBps
- Programmable output power up to 10 dBm for all supported frequencies
- Frequency range:400- 464MHz @434A type
  830 - 900 MHz @868A type
- Low current consumption (RX: 16.2 mA @1.2 kBaud,
  TX: 15.2 mA @ –6 dBm output power)
- Power down consumption:0.3uA (PM3 mode)
- Digital RSSI / LQI support
- Extend Antenna connector : MHF Type connector

MCU, Memory, and Peripherals

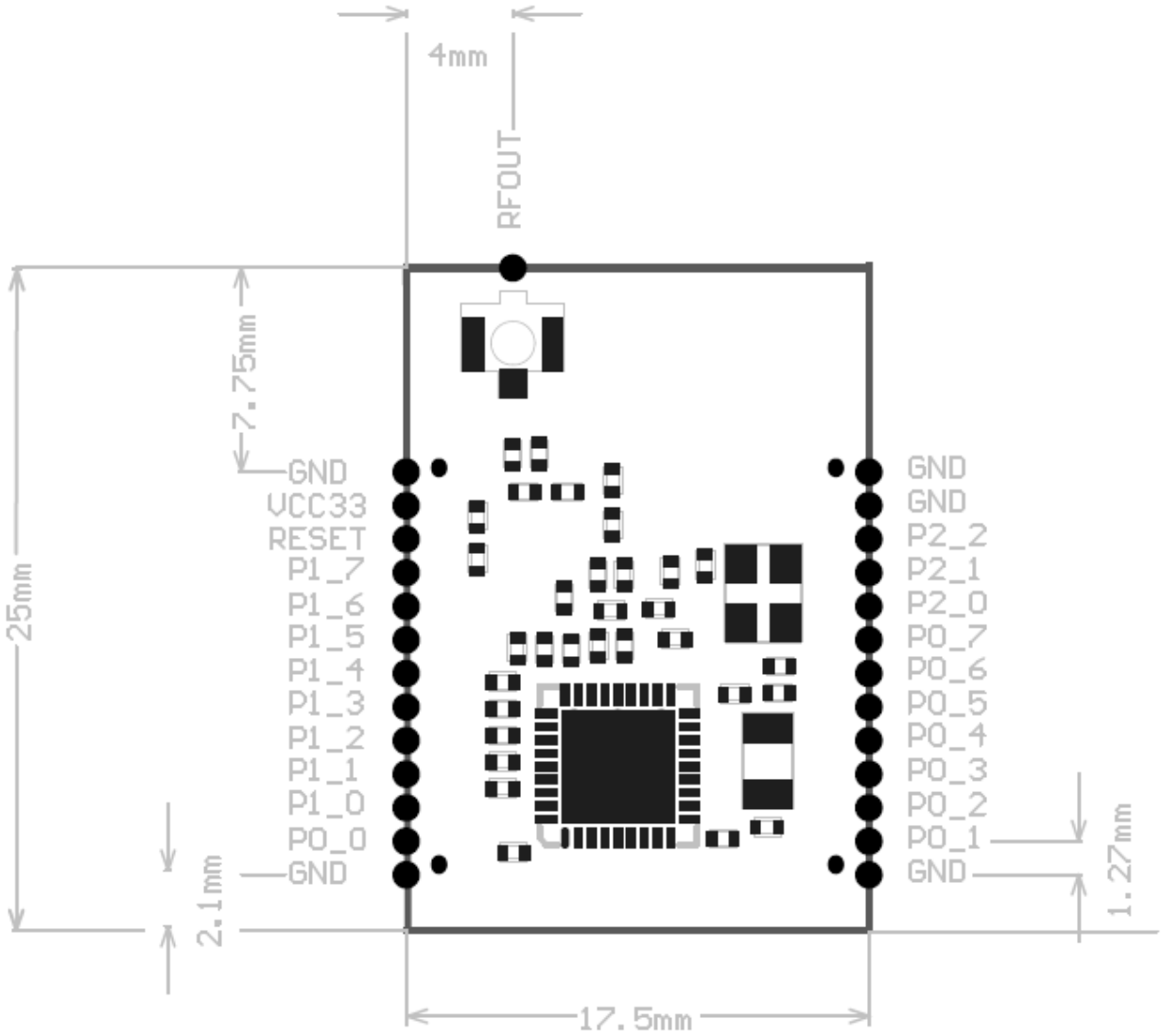
- High performance and low power 8051microcontroller core.
- Powerful DMA functionality
- 32 KB in-system programmable flash,and 4 KB RAM
- 128-bit AES security coprocessor
- 7 - 12 bit ADC with up to eight inputs
- I2S interface /two USARTs
- 16-bit timer with DSM mode / Three 8-bit timers
- 21 GPIO pins


RESET_N
RESET
WATCHDOG TIMER
ON-CHIP VOLTAGE REGULATOR
VDD (2.0 - 3.6 V)
DCOUPL
DIGITAL
ANALOG
MIXED
XOSC_Q2
XOSC_Q1
26 MHz CRYSTAL OSC
CLOCK MUX & CALIBRATION
POWER ON RESET
SFR bus
SLEEP TIMER
P2_4
P2_3
P2_2
P2_1
P2_0
32.768 kHz CRYSTAL OSC
DEBUG INTERFACE
HIGH SPEED RC-OSC
LOW PWR RC-OSC
POWER MGT. CONTROLLER
CODE
XDATA
DATA
SFR
UNIFIED
8051 CPU CORE
MEMORY ARBITRATOR
RAM
4 KB SRAM
FLASH
32 KB FLASH
DMA
IRQ CTRL
FLASH CTRL
P1_7
P1_6
P1_5
P1_4
P1_3
P1_2
P1_1
P1_0
P0_7
P0_6
P0_5
P0_4
P0_3
P0_2
P0_1
P0_0
I/O CONTROLLER
ΔΣ ADC AUDIO / DC
AES ENCRYPTION & DECRYPTION
RADIO REGISTERS
RADIO DATA INTERFACE
AGC
DEMODULATOR
SYNTH
MODULATOR
FRAME CONTROL
USART 0
USART 1
TIMER 1 (16-bit)
TIMER 2 (8-bit MAC Timer)
TIMER 3 (8-bit)
TIMER 4 (8-bit)
RECEIVE CHAIN
FREQUENCY SYNTHESIZER
TRANSMIT CHAIN
RF_P
RF_N

Pin Descriptions:

Pin	Pin name	Pin type	Description
1	GND	Ground	
2	VCC33	Power	2.0V~3.6V power supply
3	RESET	DI	Reset, active low
4	P1_7	DI/O	Port1.7
5	P1_6	DI/O	Port1.6
6	P1_5	DI/O	Port1.5
7	P1_4	DI/O	Port1.4
8	P1_3	DI/O	Port1.3
9	P1_2	DI/O	Port1.2
10	P1_1	DI/O	Port1.1
11	P1_0	DI/O	Port1.0
12	P0_0	DI/O	Port0.0
13	GND	Ground	
14	GND	Ground	
15	P0_1	DI/O	Port0.1
16	P0_2	DI/O	Port0.2
17	P0_3	DI/O	Port0.3
18	P0_4	DI/O	Port0.4
19	P0_5	DI/O	Port0.5
20	P0_6	DI/O	Port0.6
21	P0_7	DI/O	Port0.7
22	P2_0	DI/O	Port2.0
23	P2_1 (DO)	DI/O	Port2.1
24	P2_2 (DC)	DI/O	Port2.2
25	GND	Ground	
26	GND	Ground	
27	RFOUT	RF	RF output Pin

Module's dimension



Absolute Maximum Ratings

Under no circumstances must the absolute maximum ratings given in Table 2 be violated. Stress exceeding one or more of the limiting values may cause permanent damage to the device.

Parameter	Min	Max	Units	Condition
Supply voltage	–0.3	3.6	V	All supply pins must have the same voltage
Voltage on any digital pin	–0.3	VDD+0.3, max 3.6	V	
Input RF level		+10	dBm	
Storage temperature range	–50	150	°C	Device not programmed
Solder reflow temperature		260	°C	T = 10 s

Table 2: Absolute Maximum Ratings

Operating Conditions

The operating conditions for **CC1110EMS** are listed Table 3 in below.

Parameter	Min	Max	Unit	Condition
Operating ambient temperature, T_A	-40	85	°C	
Operating supply voltage	2.0	3.6	V	

Table 3: Operating Conditions

7.1 General Characteristics

T_A=25°C, VDD=3.0V if nothing else stated.

Parameter	Min	Typ	Max	Unit	Condition/Note
Wake-Up and Timing					
Power mode 1 → power mode 0 (active)		38	77	ns	Digital regulator on, High Speed RCOSC or crystal oscillator running. Entry from PM1 to PM0 takes one clock period.
Power mode 2 or 3 → power mode 0 (active)		50		µs	Digital regulator off, High Speed RCOSC and crystal oscillator off. Start-up of regulator and High Speed RCOSC.
Active → RX 26 MHz XOSC initially OFF		495		µs	Digital regulator on. Crystal oscillator off. Start-up of crystal oscillator and RF TX/RX begins.
Active → TX 26 MHz XOSC initially OFF		495		µs	Digital regulator on. Crystal oscillator off. Start-up of crystal oscillator and RF TX/RX begins.
Active → RX		195		µs	Digital regulator on. Crystal oscillator on. Time from enabling radio until RX begins.
Active → TX		195		µs	Digital regulator on. Crystal oscillator on. Time from enabling radio until TX begins.
Radio part					
Frequency range	300		348	MHz	
	400		464	MHz	
	800		928	MHz	
Data rate	1.2		500	kbps	Modulation formats supported: (Shaped) MSK (also known as differential offset QPSK) up to 500kbps 2-FSK up to 500kbps GFSK and OOK/ASK (up to 250kbps) Optional Manchester encoding (halves the data rate) Data rate must be selected to comply with frequency regulations.

Table 5: General Characteristics

Electrical Specifications(Refer to CC1110)

T_A=25° C, VDD=3.0V if nothing else stated.

Parameter	Min	Typ	Max	Unit	Condition
Power On Reset Voltage		1.1		V	Monitors the unregulated supply
Current Consumption					
MCU Active Mode, static		500		µA	Digital regulator on, High Speed RCOSC running. No radio, crystals, or peripherals.
MCU Active Mode, dynamic		270		µA/MHz	Digital regulator on, High Speed RCOSC running. No radio, crystals, or peripherals.
MCU Active Mode, highest speed		7.5		mA	MCU running at full speed (26 MHz), XOSC running. No peripherals.
MCU Active and RX Mode		22		mA	MCU running at full speed (26 MHz), XOSC running, radio in RX mode. No peripherals.
MCU Active and TX Mode, 0dBm		31		mA	MCU running at full speed (26 MHz), XOSC running, radio in TX mode. No peripherals.
Power mode 1		300		µA	Digital regulator on, High Speed RCOSC and crystal oscillator off. 32.768kHz XOSC, POR and ST active. RAM retention.
Power mode 2		0.8		µA	Digital regulator off, High Speed RCOSC and crystal oscillator off. 32.768kHz XOSC, POR and ST active. RAM retention.
Power mode 3		0.6		µA	No clocks. RAM retention. Power On Reset (POR) active.
Peripheral Current Consumption					Add to the figures above if the peripheral unit is activated
Timer 1		10		µA/MHz	When enabled
Timer 2		10		µA/MHz	When enabled
Timer 3		10		µA/MHz	When enabled
Timer 4		10		µA/MHz	When enabled
Sleep Timer		0.5		µA	Including low-power RC oscillator or 32.768kHz XOSC
AES		50		µA/MHz	When encrypting/decrypting
ADC		0.9		mA	When converting
USART1 / USART2		12		µA/MHz	For each USART in use. Not including current for driving I/O pins.
DMA		30		µA/MHz	When operating, not including current for memory access
Flash write		3		mA	

Table 4: Electrical Specifications

RF Receive Section

T_A=25° C, VDD=3.0V if nothing else stated.

Parameter	Min	Typ	Max	Unit	Condition/Note
Receiver sensitivity 315/433/868/915MHz		–109		dBm	2-FSK, 1.2kbps, 5.2kHz deviation, 1% packet error rate, 20 bytes packet length, 58kHz digital channel filter bandwidth
		–99		dBm	2-FSK, 38.4kbps, 20kHz deviation, 1% packet error rate, 20 bytes packet length, 100kHz digital channel filter bandwidth
		-87		dBm	2-FSK, 250kbps, 127kHz deviation, 1% packet error rate, 20 bytes packet length, 540kHz digital channel filter bandwidth
		-86		dBm	OOK, 250kbps OOK, 1% packet error rate, 20 bytes packet length, 540kHz digital channel filter bandwidth
Saturation		–15		dBm	
Digital channel filter bandwidth	58		812	kHz	User programmable. The bandwidth limits are proportional to crystal frequency (given values assume a 26.0MHz crystal).
Adjacent channel rejection, 868MHz		23		dB	2-FSK, 38.4kbps, 20kHz deviation, 1% packet error rate, 20 bytes packet length, 100kHz digital channel filter, 150kHz channel spacing Desired channel 3dB above the sensitivity limit.
Alternate channel rejection, 868MHz		33		dB	2-FSK, 38.4kbps, 20kHz deviation, 1% packet error rate, 20 bytes packet length, 100kHz digital channel filter, 150kHz channel spacing Desired channel 3dB above the sensitivity limit.
Image channel rejection, 868MHz		29		dB	2-FSK, 38.4kbps, 20kHz deviation, 1% packet error rate, 20 bytes packet length, 100kHz digital channel filter, 150kHz channel spacing, IF frequency 305kHz Desired channel 3dB above the sensitivity limit.
Blocking at 1MHz offset, 868MHz		52		dB	Desired channel 3dB above the sensitivity limit. Compliant to ETSI EN 300 220 class 2 receiver requirement.
Blocking at 2MHz offset, 868MHz		54		dB	Desired channel 3dB above the sensitivity limit. Compliant to ETSI EN 300 220 class 2 receiver requirement.
Blocking at 5MHz offset, 868MHz		61		dB	Desired channel 3dB above the sensitivity limit. Compliant to ETSI EN 300 220 class 2 receiver requirement.
Blocking at 10MHz offset, 868MHz		64		dB	Desired channel 3dB above the sensitivity limit. Compliant to ETSI EN 300 220 class 2 receiver requirement.
Spurious emissions			–57 –47	dBm dBm	25MHz – 1GHz Above 1GHz

Table 6: RF Receive Section

RF Transmit Section

T_A=25° C, VDD=3.0V if nothing else stated.

Parameter	Min	Typ	Max	Unit	Condition/Note
Output power, highest setting		21		dBm	Output power is programmable, and full range is available in all frequency bands. Output power must be selected to comply with frequency regulations. Delivered to a 50Ω single-ended load via Chipcon reference RF matching network.
Output power, lowest setting		-30		dBm	Output power is programmable, and full range is available in all frequency bands. Delivered to a 50Ω single-ended load via Chipcon reference RF matching network.
Spurious emissions and harmonics,			-36 -54 -47 -30	dBm	25MHz – 1GHz 47-74, 87.5-118, 174-230, 470-862MHz 1800MHz-1900MHz (restricted band in Europe), when the operating frequency is below 900MHz (2nd harmonic can not fall within this band when used in Europe) Otherwise above 1GHz
Spurious emissions,			-49.2 -41.2	dBm EIRP dBm EIRP	<200µV/m at 3m below 960MHz. <500µV/m at 3m above 960MHz.
Harmonics			-20 -41.2	dBc dBm	2nd harmonic 3rd, 4th and 5th harmonic

7.6 Low Power RC Oscillator

T_A=25°C, VDD=3.0V if nothing else is stated.

Parameter	Min	Typ	Max	Unit	Condition/Note
Calibrated frequency	34.6	34.7	36	kHz	Calibrated RC Oscillator frequency is XTAL frequency divided by 750
Frequency accuracy after calibration			+0.3 -10	%	
Temperature coefficient		+0.4		% / °C	Frequency drift when temperature changes after calibration
Supply voltage coefficient		+3		% / V	Frequency drift when supply voltage changes after calibration
Initial calibration time		2		ms	When the RC Oscillator is enabled, calibration is continuously done in the background as long as the crystal oscillator is running.
Wake-up period	58µ		59650	Seconds	Programmable, dependent on XTAL frequency

Table 10: Low Power RC Oscillator parameters

7.7 High Speed RC Oscillator

T_A=25°C, VDD=3.0V if nothing else is stated.

Parameter	Min	Typ	Max	Unit	Condition/Note
Frequency		13		MHz	Calibrated High Speed RC Oscillator frequency is XTAL frequency multiplied by 1/2
Uncalibrated frequency accuracy		±15		%	
Calibrated frequency accuracy			±1	%	
Start-up time			10	µs	
Temperature coefficient			-325	ppm / °C	Frequency drift when temperature changes after calibration
Supply voltage coefficient			28	ppm / V	Frequency drift when supply voltage changes after calibration
Initial calibration time		50		µs	When the High Speed RC Oscillator is enabled, calibration is continuously done in the background as long as the crystal oscillator is running.

Table 11: High Speed RC Oscillator parameters

#MO-CC1110F32 not include 32.768khz crystal , So need used RC mode to make lower-power application#

Frequency Synthesizer Characteristics

T_A=25° C, VDD=3.0V if nothing else stated.

Parameter	Min	Typ	Max	Unit	Condition/Note
Programmed frequency resolution	397	$F_{XOSC}/2^{18}$	412	Hz	26MHz-27MHz crystal. The resolution (in Hz) is equal for all frequency bands.
Synthesizer frequency tolerance		±40		ppm	Given by crystal used. Required accuracy (including temperature and aging) depends on frequency band and channel bandwidth / spacing.
PLL turn-on / hop time			80	µs	Time from leaving the IDLE state (see Figure 38) until arriving in the RX, FSTXON or TX state, when not performing calibration. Crystal oscillator running.
PLL RX/TX and TX/RX settling time			10	µs	Settling time for the 1xIF frequency step from RX to TX, and vice versa.
PLL calibration time	 0.69	18739 0.72	 0.72	XOSC cycles ms	Calibration can be initiated manually, or automatically before entering or after leaving RX/TX. Min/typ/max time is for 27/26/26MHz crystal frequency.

Table 12: Frequency Synthesizer Parameters

Analog Temperature Sensor

T_A=25° C, VDD=3.0V if nothing else stated.

Parameter	Min	Typ	Max	Unit	Condition/Note
Output voltage at –40°C		0.660		V	
Output voltage at 0°C		0.755		V	
Output voltage at +40°C		0.859		V	
Output voltage at +80°C		0.958		V	
Temperature coefficient		2.54		mV/°C	Fitted from –20°C to +80°C
Error in calculated temperature, calibrated		0		°C	From –20°C to +80°C when using 2.44mV / °C, after 1-point calibration at room temperature
Current consumption increase when enabled		0.3		mA	

Table 13: Analog Temperature Sensor Parameters

8-14 bit ADC

T_A=25° C, VDD=3.0V if nothing else stated.

Parameter	Min	Typ	Max	Unit	Condition/Note
Input voltage	0		AVDD	V	AVDD is voltage on AVDD pin
External reference voltage	0		AVDD	V	AVDD is voltage on AVDD pin
External reference voltage differential	0		AVDD	V	AVDD is voltage on AVDD pin
Number of bits (ENOB)	8		13	bits	The ADC is a delta-sigma. Effective resolution depends on sample rate used. Differential input signal and reference.
Offset		TBD		LSB	
Conversion time	18		114	µs	Using 26 MHz crystal oscillator
Differential nonlinearity (DNL)		±0.3		LSB	8-bits setting
Integral nonlinearity (INL)		±0.8		LSB	8-bits setting
SINAD		45		dB	8-bits setting
(sine input)		56		dB	10-bits setting
		66		dB	12-bits setting
		75		dB	14-bits setting

Table 14: 8-14 bit ADC Characteristics

Control AC Characteristics :

T_A=85° C, VDD=3.0V if nothing else stated.

Parameter	Min	Typ	Max	Unit	Condition/Note
System clock, f_{SYSCLK} t_{SYSCLK}= 1/ f_{SYSCLK}			26	MHz	Applies when the 26 MHz crystal oscillator is used. Maximum system clock is 13 MHz when high speed RC oscillator is used.
RESET_N low width	2.5			ns	See item 1, Figure 1. This is the shortest pulse that is guaranteed to be recognized as a reset pin request.
Interrupt pulse width	t_{SYSCLK}				See item 2, Figure 1.This is the shortest pulse that is guaranteed to be recognized as an interrupt request. In PM2/3 the internal synchronizers are bypassed so this requirement does not apply in PM2/3.

Table 15: Control Inputs AC Characteristics

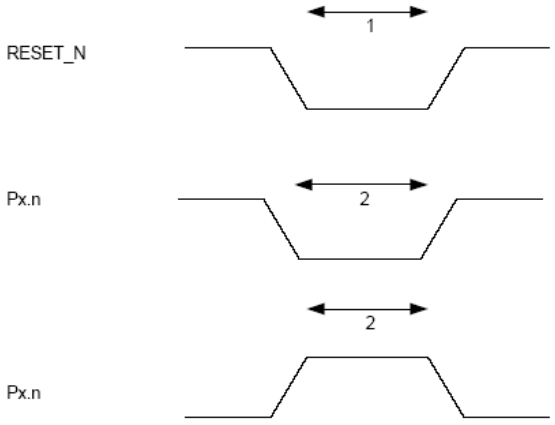


Figure 3 : Control Inputs AC Characteristics

SPI AC Characteristics :

T_A=85° C, VDD=3.0V if nothing else stated.

Parameter	Min	Typ	Max	Unit	Condition/Note
SCK period		See section 13.13.3		ns	Master. See item 1 Figure 2
SCK duty cycle		50%			Master.
MISO setup	10			ns	Master. See item 2 Figure 2
MISO hold	10			ns	Master. See item 3 Figure 2
SCK to MOSI			25	ns	Master. See item 4 Figure 2, load = 10 pF
SCK period	100			ns	Slave. See item 1 Figure 2
SCK duty cycle		50%			Slave.
MOSI setup	10			ns	Slave. See item 2 Figure 2
MOSI hold	10			ns	Slave. See item 3 Figure 2
SCK to MISO			25	ns	Slave. See item 4 Figure 2, load = 10 pF

Table 16: SPI AC Characteristics

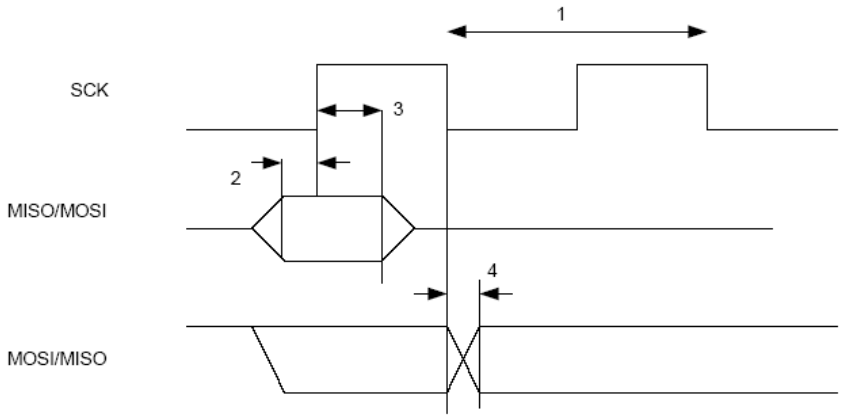


Figure 4 : SPI AC Characteristics

Debug Interface AC Characteristics :

T_A=85° C, VDD=3.0V if nothing else stated.

Parameter	Min	Typ	Max	Unit	Condition/Note
Debug clock period	31.25			ns	See item 1 Figure 3
Debug data setup	5				See item 2 Figure 3
Debug data hold	5				See item 3 Figure 3
Clock to data delay			10		See item 4 Figure 3, load = 10 pF
RESET_N inactive after P2_2 rising	10				See item 5 Figure 3

Table 17: Debug Interface AC Characteristics

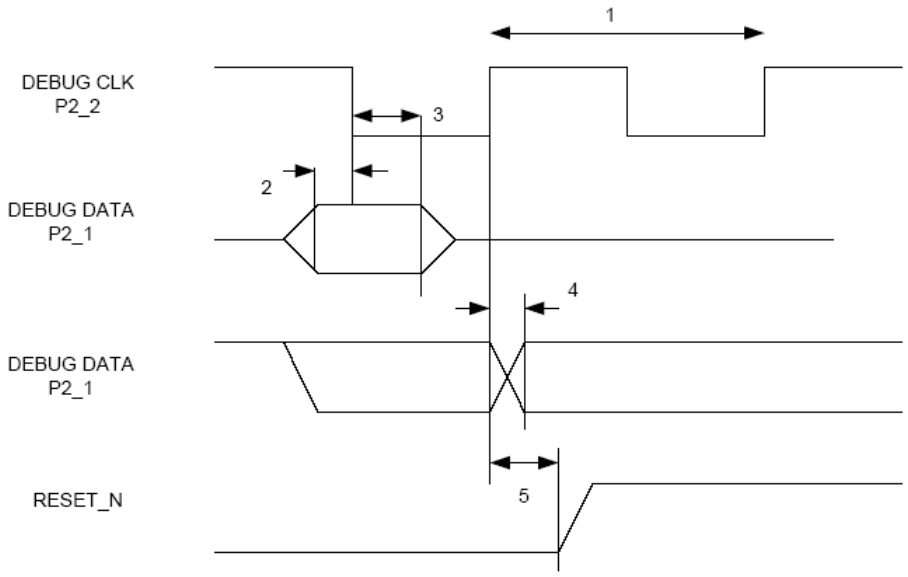


Figure 5 : Debug Interface AC Characteristics

7.14 Port Outputs AC Characteristics : T_A=85° C, VDD=3.0V if nothing else stated.

Parameter	Min	Typ	Max	Unit	Condition/Note
P0, P1, P2Port output pins, rise and fall time		10			Load = 10 pF Timing is with respect to 10% VDD and 90% VDD levels.

Table 18: Port Outputs AC Characteristics

Timer Inputs AC Characteristics

T_A =85° C, VDD=3.0V if nothing else stated.

Parameter	Min	Typ	Max	Unit	Condition/Note
Input capture pulse width	t_{SYSCLK}				Synchronizers determine the shortest input pulse that can be recognized. The synchronizers operate from the current system clock rate

Table 19: Timer Inputs AC Characteristics

DC Characteristics :

T_A=25° C, VDD=3.0V if nothing else stated.

Digital Inputs/Outputs	Min	Typ	Max	Unit	Condition
Logic "0" input voltage	0	0.7	0.9	V	
Logic "1" input voltage	VDD-0.25	VDD	VDD	V	
Logic "0" output voltage	0	0	0.25	V	For up to 4mA output current on all pins except P1_0 and P1_1 which are up to 20 mA
Logic "1" output voltage	VDD-0.25	VDD	VDD	V	For up to 4mA output current on all pins except P1_0 and P1_1 which are up to 20 mA
Logic "0" input current	N/A	–1	–1	µA	Input equals 0V
Logic "1" input current	N/A	1	1	µA	Input equals VDD
I/O pin pull-up and pull-down resistor	17	20	23	kΩ	

Table 20: DC Characteristics

CPU and Peripherals

The 8051 CPU core is a single-cycle 8051-compatible core. It has three different memory access buses (SFR, DATA and CODE/XDATA), a debug interface and an 18-input extended interrupt unit.

The memory crossbar/arbitrator is at the heart of the system as it connects the CPU and DMA controller with the physical memories and all peripherals through the SFR bus. The memory arbitrator has four memory access points, access at which can map to one of three physical memories: a 4 KB SRAM, 32 KB flash memory or SFR registers. The memory arbitrator is responsible for performing arbitration and sequencing between simultaneous memory accesses to the same physical memory.

The SFR bus is drawn conceptually in the block diagram as a common bus that connects all hardware peripherals to the memory arbitrator. The SFR bus also provides access to the radio registers in the radio register bank even though these are indeed mapped into XDATA memory space.

The 4 KB SRAM maps to the DATA memory space and part of the XDATA/CODE memory spaces. The memory is an ultra-low-power SRAM that retains its contents even when the digital part is powered off (power modes 2 and 3).

The 32 KB flash block provides in-circuit programmable non-volatile program memory for the device and maps into the CODE and XDATA memory spaces. Writing to the flash block is performed through a flash controller that allows page-wise (1024 byte) erasure and byte-wise reprogramming.

A versatile five-channel DMA controller is available in the system and accesses memory using a unified memory space (XDATA) and thus has access to all physical memories. Each channel is configured (trigger, priority, transfer mode, addressing mode, source and destination pointers, and transfer count) with DMA descriptors anywhere in memory. Many of the hardware peripherals rely on the DMA controller for efficient operation (AES core, flash write by performing data transfers between a single SFR address and flash/SRAM.

The interrupt controller services 18 interrupt sources, divided into six *interrupt groups,* each of which is associated with one of four interrupt priorities. An interrupt request is serviced even if the device is in a sleep mode (power modes 1-3) by bringing the **CC1110** back to active mode (power mode 0).

The debug interface implements a proprietary two-wire serial interface that is used for incircuit debugging. Through this debug interface it is possible to perform an erasure of the entire flash memory, control which oscillators are enabled, stop and start execution of the user program, execute
supplied instructions on the 8051 core, set code breakpoints, and single step through instructions in the code. Using these techniques, it is possible to elegantly perform in-circuit debugging and external flash programming.

The I/O-controller is responsible for all general- purpose I/O pins. The CPU can configure whether peripheral modules control certain pins or whether they are under software control, and if so whether each pin is configured as an input or output and if a pullup or pull-down resistor in the pad is connected. Each peripheral that connects to the I/O-pins can choose between two different locations to ensure flexibility in various applications.

The sleep timer is an ultra-low power timer that counts 32.768 kHz crystal oscillator or 32.768 kHz RC oscillator periods. The sleep timer runs continuously in all operating modes except power mode 3. It can be configured in one of several resolution modes, to strike the right balance between timer resolution and timeout period. Typical uses for it is as a real time counter that runs regardless of operating mode (except power mode 3) or as a wakeup timer to get out of power modes 1 or 2.

A built-in watchdog timer allows the **CC1110** to reset itself in case the firmware hangs. When enabled, the watchdog timer must be cleared periodically, otherwise it will reset the device when it times out.

Timer 1 is a 16-bit timer with timer/counter/PWM functionality. It has a programmable prescaler, a 16-bit period value and three individually programmable counter/capture channels each with a 16-bit compare value. Each of the counter/capture channels can be used as PWM outputs or to capture the timing of edges on input signals.

Timer 2 (MAC timer) is specifically designed to support time-slotted protocols in software. The timer has a configurable timer period and 18-bit tunable prescaler range.

Timers 3 and 4 are 8-bit timers with timer/counter /PWM functionality. They have a programmable prescaler, an 8-bit period value and one programmable counter/capture channel with an 8-bit compare value. Each of the counter/capture channels can be used as PWM outputs or to capture the timing of edges on input signals.

USART 0 and 1 are each configurable as either an SPI master/slave or a UART. They provide double buffering on both RX and TX and hardware flow-control and are thus well suited to high-throughput full-duplex applications. Each has its own high-precision baud-rate generator thus leaving the ordinary timers free for other uses. When configured as an SPI slave they sample the input signal using SCK directly instead of some oversampling scheme and are thus well suited to high data rates.

The AES encryption/decryption core allows the user to encrypt and decrypt data using the AES algorithm with 128-bit keys. The ADC supports 8 to 14 bits of resolution in a 30 kHz to 4 kHz bandwidth respectively. DC and audio conversion with up to eight input channels (Port 0) is possible. The inputs can be selected as single ended or differential.
The reference voltage can be internal, AVDD, or a single ended or differential external signal.

The ADC also has a temperature sensor input channel. The ADC can automate the process of periodic sampling or conversion over a sequence of channels.

Radio

CC1110 features an RF transceiver based on the industry-leading **CC1100**, requiring very few external components.

Power Control

The **CC1110** has four power modes, called PM0,PM1, PM2 and PM3. PM0 is the active mode while PM1 to PM3 are low-power modes, where PM3 has the lowest power consumption. The power modes are shown in Table 22 together with voltage regulator and oscillator options.

Power Mode	High speed oscillator	Low-speed oscillator	Voltage regulator (digital)
Configuration	A None B 26 MHz XOSC C HS RCOSC D Both	A None B Low power RCOSC C 32.768 kHz XOSC	A Off B On
PM0	B, C, D	B, C	B
PM1	A	B, C	B
PM2	A	B, C	A
PM3	A	A	A

Table 22: Power modes

PM0: The active mode. The voltage regulator to the digital core is on and either the high speed RC oscillator or the 26 MHz crystal oscillator or both are running. Either the low power RC oscillator or the 32.768 kHz crystal oscillator is running.

PM1: The voltage regulator to the digital part is on. Neither the 26 MHz crystal oscillator nor the high speed RC oscillator is running. Either the low power RC oscillator or the 32.768 kHz crystal oscillator is running. The system will go to PM0 on reset or an external interrupt or when the sleep timer expires.

PM2: The voltage regulator to the digital core is turned off. Neither the 26 MHz crystal oscillator nor the high speed RC oscillator is running. Either the low power RC oscillator or the 32.768 kHz crystal oscillator is running. The system will go to PM0 on reset or an external interrupt or when the sleep timer expires.

PM3: The voltage regulator to the digital core is turned off. None of the oscillators are running. The system will go to PM0 on reset or an external interrupt.

Ordering information :

Model Numbers	Frequency Ranges	Descriptions
MO-CC1110F32-434A	400MHz~464MHz	32KB flash memory
MO-CC1110F32-868A	830MHz~900MHz	32KB flash memory
MO-CC1110F16-434A	400MHz~464MHz	16KB flash memory
MO-CC1110F16-868A	830MHz~900MHz	16KB flash memory
MO-CC1110F8-434A	400MHz~464MHz	8KB flash memory
MO-CC1110F8-868A	830MHz~900MHz	8KB flash memory

Note : For detailed information, please see TI CC1110 data sheet .

TI WEB : www.ti.com